GENERAL DESCRIPTION

The device features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The four bus signals are a clock input (SCLK), a serial data input (SI), a serial data output (SO), and a chip select (CS#). Serial access to the device is enabled by CS# input.

When it is in Dual Output read mode, the SI and SO pins become SIO0 and SIO1 pins for data output.

The device provides sequential read operation on whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page basis, or word basis for erase command is executes on sector, or block, or whole chip basis.

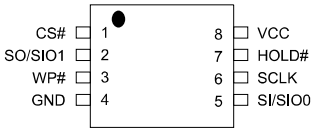
To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode.

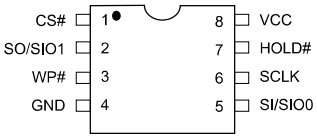
The device utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

PIN CONFIGURATIONS

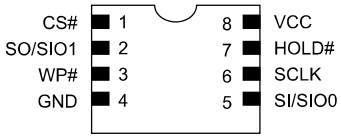
8-PIN SOP (150/200mil)



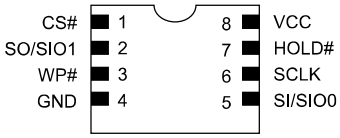
8-PIN PDIP (300mil)



8-LAND, WSON (6x5mm)



8-LAND USON (2x3mm)



PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O) / Serial Data Input & Output (for Dual Output mode)
SO/SIO1	Serial Data Output (for 1 x I/O) / Serial Data Output (for Dual Output mode)
SCLK	Clock Input
WP#	Write Protection
HOLD#	Hold, to pause the device without deselecting the device
VCC	+ 3.3V Power Supply
GND	Ground